REMARKS / ARGUMENTS

This Amendments and Response to Office Action is filed in response to the Office Action of June 28, 2005.

The disclosure is objected to because the newly added Fig. 5A allegedly lacks a description. Also, the specification is objected to because the specification allegedly fails to clearly recite that "the power-down control signal being changed to a high state for a predetermined period when the signal from the first logic family changes state" as claimed in independent claims 1, 3, 6, and 8, or that "the first transistor cuts off the connection between the level shifter unit and the power terminal when the voltage level of the input terminal of the level shift unit changes" as claimed in independent claim 11. The specification also allegedly fails to clearly claimed that "the power-down control signal being changed to a low state for a predetermined period when the signal from the first logic family changes state" as claimed in independent claim 10.

Claims 1, 11, 15, and 16 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,433,582 issued to Hirano ("Hirano"). Moreover, claims 2, 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of U.S. Patent No. 5,917,339 issued to Kim ("Kim"). Claims 4-8 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Kim and further in view of U.S. Patent No. 6,249,145 Tanaka *et al.* ("Tanaka *et al.*"). Moreover, claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Tanaka *et al.* Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano. Moreover, claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Tanaka *et al.*

With entry of the above amendments and consideration of the reasons stated below, Applicants respectfully submit that the objections and rejections set forth in the outstanding Office Action are overcome.

I. Objections of the specification

Applicants submit that with the amendment to the specification, and the reasons states below, the objections have been overcome, and their withdrawal is respectfully requested.

Specifically, the specification is objected to because the specification allegedly fails to clearly recite that "the power-down control signal being changed to a high state for a predetermined period when the signal from the first logic family changes state" as claimed in independent claims 1, 3, 6, and 8, and that "the first transistor cuts off the connection between the level shifter unit and the power terminal when the voltage level of the input terminal of the level shift unit changes" as claimed in independent claim 11

Applicants submit that the features of the subject invention include that the level shift unit cuts off power supplied to the PMOS transistors 230 during the state transition. This feature is shown in , for example, paragraph 0032: "[t]hus, in the shifter circuit apparatus of FIG. 2, the presence of this PMOS device 230 prevents the simultaneous conduction of the N- and PMOS transistors in the basic shifter circuitry 100 when level-shifting transition is taking place. The control PMOS transistor 230 serves to cut off current supply to the PMOS transistors 211 and 221 during the transition period of the NMOS transistors 212 and 222. This allows NMOS transistors 212 and 222 to operate independently from their PMOS counterparts. PMOS transistors 211 and 221 are only enabled after their corresponding NMOS transistors 212 and 222 conclude their state transition." Applicants submit that the objection has been overcome, and its

withdrawal is respectfully requested.

The specification also allegedly fails to clearly recite that "the power-down control signal being changed to a low state for a predetermined period when the signal from the first logic family changes state" as claimed in independent claim 10.

Again, in the original specification, one of the alternative embodiments, starting in paragraph 0049, states "FIG. 7 illustrated a shifter based on the concept of the invention that is suitable for converting digital signals to negative-voltage ratings. Such a shifter 700 has a circuit configuration that is substantially equivalent to the shifter 200 of FIG. 2 except that the P- and NMOS devices are swapped into ones with reverse polarity. The shifter 700, as a result, needs to be tied to a negative-valued voltage VEE2 in order to function properly and convert a low-voltage negative signal into a high-voltage negative signal." Further in paragraph 0052, "[t]he gate terminal 731 of the power-down control NMOS transistor 730 is controlled by a power-down control signal PWD to cut off the NMOS transistors 712 and 722 for a duration of time sufficient for the PMOS transistors 721 and 722 to settle their state transition. The time period, as easily understood for those skilled in the art, may be implemented in t scheme similar to that illustrated in FIG. 3." Applicants submit that the specification fully supports the invention as claimed in independent claim 10 and the objection has been overcome. Its withdrawal is respectfully requested.

II. Rejection of Claims 1, 11, 15, and 16 under 35 U.S.C. 102(e) as being anticipated by Hirano

III. Rejection of claims 2, 3 and 17 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano and Kim

IV. Rejection of claims 4-8 and 18-20 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano, Kim and Tanaka *et al.*

V. Rejection of claim 8 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano and Tanaka *et al.*

VI. Rejection of claim 10 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano

VII. Rejection of claims 12-14 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano and Tanaka *et al.*

Prior to a discussion of the Examiner's rejections made in the outstanding Office Action, it is believed that it may be beneficial to briefly review the subject application. The subject application is directed to overcome the drawbacks in a conventional level shifter circuitry when the voltage difference between the shifted signals is relatively large. To accomplish the above objective, with reference to FIGs. 2 and 3 of the subject application, the dynamic CMOS level shifter circuit apparatus uses a power-down control signal (*PWD*) at the gate terminal 231 of the PMOS transistor 230 for a specified period time during operation. More particularly, when the input signal changes state, for example, from high state to low state, the power-down control signal (*PWD*) is applied for a predetermined period. The power-down control signal (*PWD*)

will **cut off power** supplied to the PMOS transistors 211 and 221 in FIG. 2 until the NMOS transistors 212 and 222 shown in FIG. 2 settle their state transition.

In the original specification, this feature of the subject invention, that the level shift unit cuts off power supplied to the PMOS transistors 230 during the state transition, is stated in, for example, paragraph 0032, "[t]hus, in the shifter circuit apparatus of FIG. 2, the presence of this PMOS device 230 prevents the simultaneous conduction of the N- and PMOS transistors in the basic shifter circuitry 100 when level-shifting transition is taking place. The control PMOS transistor 230 serves to **cut off current supply** to the PMOS transistors 211 and 221 during the transition period of the NMOS transistors 212 and 222. This allows NMOS transistors 212 and 222 to operate independently from their PMOS counterparts. PMOS transistors 211 and 221 are only enabled after their corresponding NMOS transistors 212 and 222 conclude their state transition."

Similarly, paragraph 0049 also states that "FIG. 7 illustrated a shifter based on the concept of the invention that is suitable for converting digital signals to negative-voltage ratings. Such a shifter 700 has a circuit configuration that is substantially equivalent to the shifter 200 of FIG. 2 except that the P- and NMOS devices are swapped into ones with reverse polarity. The shifter 700, as a result, needs to be tied to a negative-valued voltage VEE2 in order to function properly and convert a low-voltage negative signal into a high-voltage negative signal." Further in paragraph 0052, "[t]he gate terminal 731 of the power-down control NMOS transistor 730 is controlled by a power-down control signal PWD to **cut off** the NMOS transistors 712 and 722 for a duration of time sufficient for the PMOS transistors 721 and 722 to settle their state transition. The time period, as easily understood for those skilled in the art, may be implemented in t scheme similar to that illustrated in FIG. 3."

The cited prior art reference Hirano fails to teach or suggest such a common feature of the object application, that is "the power-down control signal controls the gate terminal of said power-down control PMOS transistor to **cut off the power** to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition." The control signal APD of Hiraro only uses to limit the current flow in the circuitry. For example, it disclosed in column 7, lines 58-65 of the Hirano patent that "[t]he signal ATD is then caused to transition from a reference voltage Vss to a voltage Vvv, whereby an onstate **resistance** between the source and the drain of the MOS transistor PR1 **is increased**. In this case, the voltage Vvv is a voltage which is higher than a reference voltage Vss wile being lower than a voltage Vcc. Then, the input signal Si is caused to transition from a voltage Vcc to a reference voltage Vss." It also disclosed in column 8, lines 4-8 of the Hirano patent that, "[i]n the second example, when the input signal Si transitions from a voltage Vcc to a reference voltage Vss, the **current driving capability** of the MOS transistor PR1 is **degraded**, and therefore a **resistance** between the source and drain of the MOS transistor PR1 is **increased**." The remaining cited prior art references Kim and Tanaka et al. also fail to teach or suggest such a common feature.

Reconsideration of all the independent claims 1, 3, 6, 8, 10, and 11 are therefore respectfully requested.

As the rejected dependent claims 2, 4-5, 7, and 12-20 depend upon their respective independent claims 1, 3, and 11 and in view that the independent claims 1, 3, 6, 8, 10 and 11 are allowable, reconsideration of the rejections over claims 2, 4-5, 7, and 12-20 are therefore requested.

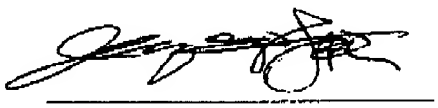
With regard to above arguments, the withdrawal of this rejection is respectfully solicited.

CONCLUSION

For at least the foregoing reasons, it is believed that all of pending claims 1-8 and 10-20 of the present application patently define over the prior art references and are in proper condition for allowance. Furthermore, because no new claim is added, no additional fees are required. In the event, however, that additional fees are required to complete this filing, Commissioner is authorized to deduct any deficiencies from Deposit Account 13-0480, Attorney Docket No. 87157656.242004.

If the Examiner has any questions regarding this filing or the application in general, the Examiner is invited to contact Applicants' attorney at the below-listed telephone number.

Respectfully submitted,



Date: October 27, 2005

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